Code No: R31042 **R10** **Set No: 1**

III B.Tech. I Semester Supplementary Examinations, June/July - 2014

DIGITAL IC APPLICATIONS

(Comm to ECE, EIE, BME, ECC)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the operation of the CMOS AND OR INVERT gate with neat sketches and draw the functional table.
   (b) What do you mean by current spikes? Explain the need of decoupling and filtering capacitors?

2. (a) What are the different factors considered in TTL/CMOS interfacing? Explain.
   (b) Explain the logic levels and noise margins of TTL.

3. (a) Explain 74x280 9-bit parity generator? Also explain how a parity circuit might be used to detect errors in memory of the micro processor system.
   (b) Explain the 8-bit comparator using 74x682.

4. (a) Explain the different functions performed by the 74x181 4-bit ALU.
   (b) What is a combinational multiplier? Draw the interconnections for an 8x8 combinational multiplier.

5. (a) What is synchronous design methodology? Explain the synchronous system structure with a block diagram and operations performed during one clock cycle.
   (b) Explain how to convert JK flip-flop to T flip-flop and D flip-flop with excitation table, logic diagram and K map simplification.

6. (a) Design a 4 bit, 8 states Johnson counter using IC 74x194. Show how the same counter can be modified as a self correcting Johnson counter.
   (b) What are the basic design steps of a sequential logic? Explain.

7. (a) Compare PROM, PLA and PAL.
   (b) Implement the following Boolean functions using PAL.
   $w(A,B,C,D)= \sum m(0,2,6,7,8,9,12,13)$
   $x(A,B,C,D)= \sum m(0,2,6,7,8,9,12,13,14)$
   $y(A,B,C,D)= \sum m(2,3,8,9,10,12,13)$
   $z(A,B,C,D)= \sum m(1,3,4,6,9,12,14)$

8. (a)Draw the internal structure of synchronous SRAM and explain the operating modes of SSRAM.
   (b) Explain the 2 dimensional decoding technique.

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Code No: R31042 **R10** **Set No: 2**

III B.Tech. I Semester Supplementary Examinations, June/July - 2014

DIGITAL IC APPLICATIONS

(Comm to ECE, EIE, BME, ECC)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) What is the difference between static and dynamic power dissipation? Derive an expression for total dynamic power dissipation of CMOS circuit.
   (b) Explain the CMOS inverter circuit behavior with resistive loads.

2. (a) Contrast between TTL, CMOS, and ECL logic families.
   (b) Explain the operation of the two input LS-TTL NAND gate with neat circuit diagrams. Also define the sinking current and sourcing currents.

3. (a) Design a 5 to 32 decoder using 74x138's and a 74x139.
   (b) Explain about the three state buffers.

4. (a) Explain a simple floating point encoder? Explain how a 11 bit fixed point integer B can be converted in to a 7 bit floating point number.
   (b) Explain the 4 bit Ripple adder with neat diagrams.

5. (a) Explain the functional and internal behavior of master slave JK flip-flop.
   (b) Explain the impediments of a synchronous design.

6. (a) What are the modes of operation of the shift registers? Explain.
   (b) Design a modulus 5 synchronous counter using the JK flip flop and also construct the timing diagram.

7. (a) Distinguish the PAL with PLA.
   (b) Implement the following functions with PLA.
   $A(x,y,z)= \sum m(1,2,4,6)$
   $B(x,y,z)= \sum m(0,1,6,7)$
   $C(x,y,z)= \sum m(2,6)$

8. (a) Explain the types of the ROM? Also list the applications of it.
   (b) Explain the timing of DRAM with neat timing diagrams.

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Code No: R31042 **R10** **Set No: 3**

III B.Tech. I Semester Supplementary Examinations, June/July - 2014

DIGITAL IC APPLICATIONS

(Comm to ECE, EIE, BME, ECC)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the CMOS logic families and compare them.
   (b) Explain the following terms with respect to CMOS logic.
   (i)Fan out (ii) Fan in (iii) Propagation delay (iv) DC noise margin.

2. (a) Explain the transistor logic inverter with neat sketches. Also draw the switch mode for the transistor inverter.
   (b) Give the characteristics of ECL family. Also explain the logic levels of ECL 10K family.

3. (a) What is an iterative circuit? Explain iterative comparator circuit.
   (b) Design a 32 to 1 multiplexer using 8x1 multiplexer.

4. (a) Explain the carry look ahead adder. Also obtain the carry equation for the first four adder stages.
   (b) What is a dual priority encoder? Explain the design considerations of it.

5. (a) Explain the different types of the SSI latches and flip-flops.
   (b) Explain the applications of the counter.

6. (a) Design a modulus 5 synchronous counter using the JK flip flop and also construct the timing diagram.
   (b) What is a universal shift registers. Draw the logic diagram and functional table for 74x194 4 bit universal shift register.

7. (a) Tabulate the PLA Programmable table for the four Boolean functions listed below
   $A(x,y,z)= \sum m(1,2,4,6)$
   $B(x,y,z)= \sum m(0,1,6,7)$
   $C(x,y,z)= \sum m(2,6)$
   $D(x,y,z)= \sum m(1,2,3,5,7)$
   (b) What is PAL? Explain the array logic for typical PAL with diagram.

8. (a) Explain the read and write cycle timings of SRAM.
   (b) Contrast between PROM, EPROM and EEPROM.

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Code No: R31042 **R10** **Set No: 4**

III B.Tech. I Semester Supplementary Examinations, June/July - 2014

DIGITAL IC APPLICATIONS

(Comm to ECE, EIE, BME, ECC)

Time: 3 Hours **Max Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1. (a) Explain the CMOS dynamic electrical behavior with neat sketches and necessary equations.
   (b) Explain the CMOS logic levels.

2. (a) Explain the operation of a 2-input AND gate using the diode logic with neat circuit diagrams.
   (b) Compare the totem pole and open collector outputs of a TTL

3. (a) Draw the logic symbol, truth table and logic diagram of a 74x148 priority encoder? Explain.
   (b) Explain about the three state buffers.

4. (a) Explain the operation of the 16-bit barrel shifter.
   (b) Explain about the cascading comparators and design considerations of it.

5. (a) What is a bistable element? Explain the digital and analog analysis of bistable.
   (b) Explain the setup time, hold time, Propagation delay and minimum pulse width with respect to flip flops.

6. (a) Explain the modes of operations of a shift registers with neat sketches.
   (b) Draw the basic circuit, timing diagram and different states of a 4-bit Johnson counter with a neat diagram.

7. (a) What is PAL? Compare PAL with PLA.
   (b) Implement the following multi Boolean function using 3x4x2 PLA
   $A(x,y,z)= \sum m(0,1,3,5)$ and $B(x,y,z)= \sum m(3,5,7)$

8. (a) Compare the static and dynamic RAM's.
   (b) Explain the 2D-Decoding technique.

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